REMARKS

In the Office Action the Examiner noted that claims 1-8, 11-13, and 15-16 are pending in the application, and the Examiner rejected all claims. By this Amendment, claims 1 and 16 have been amended. The Examiner's rejections are traversed below, and reconsideration of all rejected claims is respectfully requested.

Claims Rejected Under 35 USC §102

In items 1-2 on pages 2-3 of the Office Action, the Examiner rejected claim 16 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Number 5,930,508, issued to Faraboshci et al. (hereinafter referred to as "Faraboschi").

In regard to claim 16, the Examiner cites Faraboshci as teaching;

> a parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information, said parallel processor comprising (Faraboschi figures 4 and 5 abstract column 3 lines 16-25), said parallel processor comprising:
>
> [a] plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel (Faraboschi figure 1 abstract column 3 lines 16-20 column 4 lines 46-48);
>
> [an] instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information (Faraboschi figure 7 column 3 lines 16-25 column 7 lines 32-36, the alignment logic 720 acts as the fetch unit);
>
> [a]n interface having effective bits corresponding to the instruction execution units, the effective bits indicating the corresponding instruction execution unit for each instruction word (Faraboschi column 3 lines 25-32, column 4 line 57-column 5 line 11;
>
> [w]herein the instruction words fetched by the instruction fetch unit have no attached dispersal information (Faraboschi – column 3 lines 15-25; the delimiter information is part of the instruction words and therefore is not attached to the instruction words, but is simply a part of the instruction words.)

Faraboschi discloses using instruction words which include dispersal codes, along with the operation and delimiter codes, to route the instruction words to a corresponding functional unit in a processor (Column 3, lines 15-32). This is accomplished by "generating a dispersal code for each identified word, where the dispersal code corresponds to a field of the instruction occupied by the identified word....and storing each identified word along with the corresponding dispersal and delimiter codes" (Column 3, lines 3-11). The code words, including the corresponding dispersal codes, are then stored in a memory to be retrieved by the processor (Column 3, lines 11-15). Thus, the instruction words gathered and executed by the processor in

Faraboshci contain dispersal codes along with the executable instruction and delimiter codes.

Claim 16 of the present application, as amended, recites "the instruction words fetched by the instruction fetch unit have no attached dispersal information, and the effective bits are based on an instruction word format indicating an arrangement of the basic instructions." Therefore, the effective bits are base on the format, i.e., the arrangement, of the basic instructions, and there is no need to include dispersal information along with the basic instructions.

This is in direct contrast with Faraboschi, which discloses a processor retrieving from a memory instruction words that contain dispersal codes along with the operation and delimiter codes. As stated by the Examiner in the Office Action, the dispersal information "is simply a part of the instruction words." This extra data included in the instruction words is not needed in the parallel processor of claim 16 of the present application. Further, Faraboschi does not disclose effective bits "based on an instruction word format indicating an arrangement of the basic instructions.

Accordingly, it is respectfully submitted that Faraboschi does not disclose every element of the Applicants' claim 16. In order for a document to anticipate a claim, the document must teach each and every element of the claim (MPEP §2131). Therefore, since Faraboschi does not teach the features recited in independent claim 16, as stated above, it is respectfully submitted that claim 16 patentably distinguishes over Faraboschi, and withdrawal of the §102(b) rejection is earnestly and respectfully solicited.

Claim Rejections Under 35 USC §103

In items 3-14 on pages 3-8 of the Office Action the Examiner rejected claims 1-6, 11-13, and 15 under 35 U.S.C. §103(a) as being unpatentable over Faraboschi in view of U.S. Patent No. 5,881,307, issued to Park et al. (hereinafter referred to as "Park").

The Examiner states that Faraboschi discloses "[a]n instruction issue unit recognizing and, in accordance therewith, selectively [issuing] each of the basic instructions supplied from the instruction fetch unit to one of the corresponding instruction execution units to execute the issued basic instruction (Faraboschi column 3 lines 25-32, column 4 line 57-column 5 line 11)," and that "the instruction issue unit comprises a conversion unit to generate an interface having instruction information based on the instruction words, the instruction information indicating a type of the corresponding instruction execution units (Faraboschi – column 3 lines 15-25; the

delimiter information is part of the instruction words)." The Applicants respectfully disagree with the Examiner's reading of Faraboschi.

Claim 1 of the present application, as amended, recites "a conversion unit to generate an interface having effective bits based on an instruction word format, the effective bits indicating availability of the corresponding instruction execution units and the instruction word format indicating an arrangement of the basic instructions." As these effective bits are based on the instruction word format, i.e., the arrangement of the basic instructions (as illustrated in Figure 9 of the present application), there is no need for dispersal information to be included in the instruction words. Thus, a corresponding execution unit is selected for execution of each of the basic instructions by use of the arrangement of the basic instructions.

This is in direct contrast to Faraboschi, which discloses a method in which a processor reads instructions words from a memory, and uses dispersal codes included in those instruction words to route the instruction words to corresponding functional units within the processor (Column 3, lines 1-32, Column 4, line 57 through Column 5, line 4). Because dispersal information is already included in the instruction words read from the memory, there is no need for "a conversion unit to generate an interface having effective bits based on an instruction word format, the effective bits indicating availability of the corresponding instruction execution units and the instruction word format indicating an arrangement of the basic instructions." No instruction information is generated, because the instruction words already include all the routing information needed by including the dispersal codes. Rather than disclosing this conversion unit, Faraboschi simply discloses "[a] dispersed instruction buffer [that] stores an executable instruction, wherein the executable instruction includes an operational field corresponding to each one of the plurality of functional units" (Column 3, lines 25-28). "After a compacted instruction is fetched, dispersal hardware uses the dispersal bits for each syllable to route the syllable to its corresponding functional unit" (Column 4, line 66 through Column 5, line 2). This requires excessive hardware such as a crossbar switch. Each of the basic instructions in Faraboschi is provided with these dispersal codes. For example, when two integer execution units are provided in Faraboschi, each of the basic instructions are provided with the dispersal code indicative of which one of the integer execution units is to be used for each of the respective basic instructions. Claim 1 of the present application does not need to provide such dispersal codes, since an arrangement of the basic instructions determines which of the execution units is to be used.

For at least these reasons, the disclosure of Faraboschi is in direct contrast to claim 1 of

the present application, which recites "a conversion unit to generate an interface having effective bits based on an instruction word format, the effective bits indicating availability of the corresponding instruction execution units and the instruction word format indicating an arrangement of the basic instructions." The instruction information in the generated interface allows the processor of the present application to issue instructions to corresponding instruction execution units without the requirement of dispersal information being included in the instruction words, which conserves space in the memory device which stores the instruction words. Also, because the interface supplied in the present application makes it possible to specify a selection of the instruction execution units to which the basic instructions are to be issued without including dispersal codes in the instruction words, hardware size and requirements are reduced in the processor.

Referring to claim 1, it is respectfully submitted that Faraboschi does not disclose "a conversion unit to generate an interface having effective bits based on an instruction word format, the effective bits indicating availability of the corresponding instruction execution units and the instruction word format indicating an arrangement of the basic instructions." Further, this deficiency in Faraboschi is not cured by Park. Therefore, it is respectfully submitted that claim 1 patentably distinguishes over the cited references, and withdrawal of the §103(a) rejection is requested.

Claims 2-6, 11-13, and 15 depend from claim 1 and include all of the features of that claim plus additional features which are not taught or suggested by the cited references. Therefore, it is respectfully submitted that claims 2-6, 11-13, and 15 also patentably distinguish over the cited references.

In items 15-17 on pages 8-10 the Examiner rejected claims 7-8 under 35 U.S.C. §103(a) as being unpatentable over Faraboschi in view of Park in further view of Nair et al, "Exploiting Instruction Level Parallelism in Processors by Caching Scheduled Groups" (hereinafter referred to as "Nair").

As previously discussed in this Amendment, Faraboschi does not disclose "a conversion unit to generate an interface having effective bits based on an instruction word format, the effective bits indicating availability of the corresponding instruction execution units and the instruction word format indicating an arrangement of the basic instructions," as recited in claim 1 of the present application. This deficiency in Faraboshci is not cured by Park or Nair. Further, claims 7-8 depend from claim 1 and include all of the features of that claim plus additional features which are not taught or suggested by the cited references. Therefore, it is respectfully

submitted that claims 7-8 also patentably distinguish over the cited references.

Summary

In accordance with the foregoing, claims 1 and 16 has been amended. Thus, claims 1-8, 11-13, and 15-16 are pending and under consideration.

There being no further outstanding objections or rejections, it is respectfully submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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